ABSTRACT

A programmable logic device is described having an internal three-statable bus and a plurality of driving elements coupled to the internal three-statable bus. Each of the driving elements is operable to drive the internal three-statable bus. The programmable logic device also includes a plurality of interface logic circuits with each of the plurality of interface logic circuits coupled to a different one of the plurality of driving elements. Each interface logic circuit is operable to determine whether the internal three-statable bus is being driven and the interface logic circuits are collectively operable to prevent contention of signals on the internal three-statable bus.